

## PENDING CLAIMS AND STATUS THEREOF

1. **(currently amended):** An ESD-protection structure, comprising:
  - an integrated circuit having a lighter doped p-silicon well (P- well), wherein the P- well is coupled to a common power supply rail;
    - a lighter doped n-silicon well (N- well) in the P- well;
    - a plurality of heavier doped p-silicon diffusions (P+ diffusions) in the N- well;
    - a first heavier doped n-silicon diffusion (N+ diffusion) in the N- well, wherein the first N+ diffusion surrounds the plurality of P+ diffusions and overlaps the N- well into the P- well;
    - a second heavier doped n-silicon diffusion (N+ diffusion) in the P- well, wherein the second N+ diffusion surrounds the first N+ diffusion;
    - a bond pad connected to the plurality of P+ diffusions; and
    - a connection to the second N+ diffusion.
2. **(original):** The ESD-protection structure of claim 1, wherein the P- well is the integrated circuit substrate.
3. **(original):** The ESD-protection structure of claim 1, further comprising a field oxide located between the first and second N+ diffusions.
4. **(original):** The ESD-protection structure of claim 1, further comprising a lighter doped n-silicon substrate (N- substrate) of the integrated circuit, wherein the P- well is in the N- substrate.

5. (original): The ESD-protection structure of claim 1, wherein the plurality of P+ diffusions are stripe shaped.

6. (original): The ESD-protection structure of claim 1, wherein the plurality of P+ diffusions are rectangular shaped.

7. (original): The ESD-protection structure of claim 1, wherein the plurality of P+ diffusions are square shaped.

8. (original): The ESD-protection structure of claim 1, wherein the bond pad is connected to the plurality of P+ diffusions with a first plurality of conductive vias.

9. (original): The ESD-protection structure of claim 1, wherein the connection to the second N+ diffusion is with a second plurality of conductive vias.

10. (original): The ESD-protection structure of claim 8, wherein the first plurality of conductive vias are metal.

11. (original): The ESD-protection structure of claim 8, wherein the first plurality of conductive vias comprise conductive semiconductor silicon.

12. (original): The ESD-protection structure of claim 9, wherein the second plurality of conductive vias are metal.

13. (original): The ESD-protection structure of claim 9, wherein the second plurality of conductive vias comprise conductive silicon.

14. (original): The ESD-protection structure of claim 1, further comprising a second connection to the first N+ diffusion with a third plurality of conductive vias.

15. **(currently amended):** The ESD-protection structure of claim 1, wherein the common power supply rail [[P- well]] is coupled to ground.

Claim 16 (canceled)

17. (original): The ESD-protection structure of claim 1, wherein the plurality of P+ diffusions, the first N+ diffusion and the N- well are located substantially under the bond pad.

18. **(currently amended):** An ESD-protection structure, comprising:

an integrated circuit having a lighter doped p-silicon well (P- substrate), wherein the P- well is coupled to a common power supply rail;

a lighter doped n-silicon well (N- well) in the P- substrate;

a plurality of heavier doped p-silicon diffusions (P+ diffusions) in the N- well, wherein the plurality of P+ diffusions are rectangular shaped;

a first heavier doped n-silicon diffusion (N+ diffusion) in the N- well, wherein the first N+ diffusion surrounds the plurality of P+ diffusions and overlaps the N- well into the P- well;

a second heavier doped n-silicon diffusion (N+ diffusion) in the P- substrate, wherein the second N+ diffusion surrounds the first N+ diffusion;

a field oxide located between the first and second N+ diffusions;

a bond pad connected to the plurality of P+ diffusions; and

a connection to the second N+ diffusion.

19. (original): The ESD-protection structure of claim 18, wherein the bond pad is connected to the plurality of P+ diffusions with a first plurality of conductive vias.

20. (original): The ESD-protection structure of claim 18, wherein the connection to the second N+ diffusion is with a second plurality of conductive vias.

21. (original): The ESD-protection structure of claim 19, wherein the first plurality of conductive vias are metal.

22. (original): The ESD-protection structure of claim 19, wherein the first plurality of conductive vias comprise conductive semiconductor silicon.

23. (original): The ESD-protection structure of claim 20, wherein the second plurality of conductive vias are metal.

24. (original): The ESD-protection structure of claim 20, wherein the second plurality of conductive vias comprise conductive semiconductor silicon.

25. (**currently amended**): The ESD-protection structure of claim 18, wherein the common power supply rail [[P- well]] is coupled to ground.

Claim 26 (canceled)

27. (original): The ESD-protection structure of claim 18, wherein the plurality of P+ diffusions, the first N+ diffusion and the N- well are located substantially under the bond pad.

Claim 28 (canceled)